REMARKS

Claims 45, 46, 50-52, 54, 56, 59, 60, 68-70, 73, 74 and 77 are pending in this application. Claim 73 has been amended. No new matter has been introduced. Applicant acknowledges with appreciation the allowance of claims 45, 46, 50-52 and 68-70.

Claims 54, 56, 59, 60, 73 and 74 stand rejected under 35 U.S.C. § 112, first and second paragraph, on the basis that the term "a doping concentration of said area of said substrate" in claim 73 "appears wrong." (Office Action at 2). Independent claim 73 has been amended to recite that the semiconductor substrate has "a first doping concentration" and that "said increased doping concentration" of the implanted region is "higher than said first doping concentration of said substrate" correcting, therefore, any perceived indefiniteness. Applicant respectfully submits that all pending claims are now in full compliance with 35 U.S.C. § 112.

Claims 54, 56, 73, 74 and 77 stand rejected under 35 U.S.C. § 103 as being unpatentable over Schuegraf et al. (U.S. Patent No. 5,702,976) ("Schuegraf") in view of Kooi et al. (U.S. Patent No. 3,755,001) ("Kooi") and Joo et al. (U.S. Patent No. 5,841,163) ("Joo"). This rejection is respectfully traversed.

The claimed invention relates to isolation trenches formed of two dielectric materials. As such, amended independent claim 73 recites a memory device comprising *inter alia* "a field isolation region" separating a plurality of active regions and including "an isolation trench." Amended independent claim 73 further recites that the isolation trench includes "a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls." Amended independent claim 73 also recites "an ion implanted region provided below said second area having an increased doping concentration in an area of said substrate between said separated active regions, said increased doping concentration being higher than said first doping concentration of said substrate." Amended independent claim 73 further recites that "substantially all ions from said ion

implanted region which increase said doping concentration are displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material, wherein the sidewall thickness of said first area is less than about forty percent the width of the isolation region."

Schuegraf relates to "a trench isolation process which alleviates the problem of void formation during dielectric refill." (Col. 2, lines 49-51). According to Schuegraf, "recesses (22) preferably having a trench profile" are formed by removing portions of a semiconductor substrate 10. (Col. 2, lines 60-61; Figure 3A). Schuegraf teaches that "[t]he trenches (22) are then refilled with a material (26) having a dielectric constant lower than the dielectric constant of silicon dioxide." (Col. 2, lines 61-63; Figure 3D). To avoid contamination of substrate regions adjacent to trenches 22, Schuegraf further teaches that "it is preferable to form a barrier layer 24 over the trenches 22 prior to dielectric refill." (Col. 5, lines 9-12; Figure 3B). In this manner, by "utilizing dielectric materials having a lower dielectric constant than used in the prior art," the shallow trench isolation of Schuegraf "maintains effective device isolation." (Col. 4, lines 37-40).

Kooi relates to a method of fabricating semiconductor devices having selective doping and selective oxidation. (Title; Col. 1, lines 4-11). As part of the fabrication of "a target plate (1) for converting electromagnetic radiation into electric signals," Kooi teaches that grooves 4 formed into plate 1 of n-type silicon "are covered with a layer 5 of silicon oxide which at the bottom of the grooves adjoins a surface zone 6 of n-type silicon having higher doping that the region 1." (Col. 6, lines 9-20; Figures 1-2).

Joo relates to integrated circuit structures having wide and narrow channel stop layers which are formed by employing a first and second field insulation layers coupled with a first and second channel stop impurity layers. (Col. 3, lines 38-47). For example, Joo discloses that impurity ions are implanted below the first field oxide layer and are diffused by a thermal process to form a second channel stop impurity layer. (Col. 6, lines 36-50; Figure 15).

The subject matter of claims 54, 56, 73, 74 and 77 would not have been obvious over Schuegraf in view of Kooi and Joo. Indeed, the Office Action fails to establish all elements of a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, three requirements must be met: (1) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine reference teachings; (2) a reasonable expectation of success; and (3) the prior art reference (or references when combined) must teach or suggest all the claim limitations. More importantly, the teaching or suggestion to make the claimed combination and the reasonable expectation for success must both be found in the prior art and not based on Applicant's disclosure. See, e.g., In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). The Examiner has the burden of producing a *prima facie* case of obviousness.

First, not all claim limitations are taught or suggested by the prior art, whether considered alone or in combination. None of Schuegraf, Kooi and Joo teaches or suggest trenches separating "a plurality of doped active regions" and having a first and a second areas filled with corresponding dielectric materials as well as "an ion implanted region . . . below said second area . . . *substantially all ions from said ion implanted region* . . . displaced away from said active regions *by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material, and wherein the sidewall thickness of said first area is less than about forty percent the width of the isolation region*," as amended independent claim 73 recites (emphasis added).

Schuegraf discloses trenches which are "refilled with a dielectric material" with low dielectric constant and which may be lined with a barrier layer 24 prior to the dielectric refill. (Col. 3, lines 61-62). However, Schuegraf does not teach or suggest an ion implanted region directly below the second dielectric area, as in the claimed invention. Schuegraf is also silent about any ions from an ion implanted region "being displaced away from" the active regions, as independent claim 73 recites. In fact, Schuegraf does not even

mention the existence of active regions in the "Detailed Description," or illustrate any such active regions in the "Drawings."

Kooi also does not disclose an isolation trench or "a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls," as amended independent claim 73 recites. Further, Kooi does not disclose "an ion implanted region" located "below said second area," as amended independent claims 73 recites. Kooi is also silent about the ion displacement limitations of claim 73. As shown in Figures 8 and 10 of Kooi, the ion implanted regions 6 and 28 are in contact with the dielectric materials 5 and 29, respectively, but these dielectric materials are simply not part of an isolation trench.

Joo also fails to disclose an isolation trench, much less first and second areas filled with first and second dielectric materials, or an ion implanted region below the second area, or that substantially all ions in the implanted region are displaced away from the separated active regions, as amended independent claim 73 recites. Joo teaches a "first channel stop impurity layer 67" formed beneath the second field oxide layer 66 and "a second channel stop impurity layer 68 beneath the first field oxide layer 65." (Col. 6, lines 1-3; 35-37; Figure 15). In Joo, however, the first and second channel stop impurity layers and the first and second field oxide layers are not part of an isolation trench, much less of an isolation trench filled with first and second dielectric materials, as in the claimed invention.

Second, a person of ordinary skill in the art would not have been motivated to combine Schuegraf with Kooi or Joo, as the Office Action asserts. (Office Action at 2-4). Applicant notes that courts have generally held that "[I]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for

which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108 (Fed. Cir. 1987). Accordingly, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573.

In the present case, a person of ordinary skill in the art would not have been motivated to combine Schuegraf with either Kooi or Joo. As noted above, the crux of Schuegraf is the formation of trenches that are "refilled with a material having a dielectric constant lower than the dielectric constant of silicon dioxide which is about 3.9" to "address the requirements of different integrated circuit types such as NMOS, CMOS." (Col. 2, lines 61-63). Since Schuegraf employs a low-dielectric constant material for its trenches, Schuegraf teaches that a preferred embodiment "incorporates a diffusion barrier layer lining the trench so as to prevent dopant migration into the silicon substrate." (Col. 4, lines 54-57). Schuegraf also teaches that "the trenches of the present invention are about 200 nm deep, shallower than the prior art by about 20%." (Col. 5, lines 6-8).

On the other hand, Kooi relates to an "inset oxide pattern" of a "target plate for converting electromagnetic radiation into electric signal" to be used in diode structures. (Col. 6, lines 9-16). Specifically, Kooi teaches a particular method for inset oxide pattern formation to "adjoin[s] a doped zone only at the edge." (Col. 12, lines 16-20). According to Kooi, groves (4) are first formed "of approximately 5 μm deep" (col. 7, line 23) and then surface zone (6) is implanted to "a depth of approximately 1.5 μm." (Col. 7, lines 51-52). Accordingly, a person skilled in the art would not have been motivated to combine Schuegraf, which teaches the formation of trenches "about 200 nm [2,000 Angstroms] deep, shallower than the prior art by about 20%," with Kooi, which teaches trenches more than 20 times deeper than Schuegraf, that is "of approximately 5 μm [50,000 Angstroms] deep." In addition, a person skilled in the art would not have been motivated to combine Schuegraf, which addresses requirements of NMOS and PMOS transistors, with Kooi, which addresses requirements of target plates in diode structures, particularly preventing connection between diodes. Furthermore, a person skilled in the

art would not have been motivated to combine Schuegraf, the crux of which is the formation of a shallow trench for isolation with a reduced depth and without void formation but with a barrier layer, with Kooi, the crux of which is the formation of a particular oxide inset pattern obtained by a specific method which involves using a freely projecting edge part of a mask after removal of material and without a barrier layer.

A person skilled in the art would also not have been motivated to combine Schuegraf with Joo. As noted above, Schuegraf relates to the formation of a shallow trench for isolation with a reduced depth and without void formation for MOS technology. (Col. 1, lines 31-35). Schuegraf specifically mentions that the devices are being "primarily NMOS and PMOS transistors." (Col. 1, lines 34-35). On the other hand, Joo relates to channel stop layers for flash memory cells. In fact, Joo describes its invention with relation to a NAND type flash EEPROM. (Col. 3, lines 54-56). Thus, again, a person skilled in the art would not have been motivated to combine Schuegraf, which teaches the formation of trenches "about 200 nm deep" having a low-dielectric constant material and a barrier layer in NMOS and PMOS transistors, with Joo, which teaches channel stop layers in flash memory cells.

For at least the reasons above, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 54, 56, 73, 74 and 77 is respectfully requested. Allowance of the application is solicited.

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Respectfully submitted,

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